REMARKS

Claims 1, 7, 9 to 12, 15, 17 to 19, 21, 22, 25, 27, 91, 96 to 99, 101 to 103, 108 to 114 and 116 to 139 are pending for examination in the present application, with Claims 1, 9, 15 and 129 being the pending independent claims. Claims 1, 9 to 12, 15, 22, 29, 97, 119, 126, 129 to 132 and 136 are amended herein. Claims 4, 29, 30 and 115 were previously withdrawn. No new Claims are added, and no Claims have been newly canceled. No new matter is believed to be added herein. Entry hereof and early passage to issue are respectfully requested.

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Claim Rejections – 35 USC § 103

Claims 1, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 91, 96-99, 101-103, 108-114 and 116-139 are rejected under 35 USC § 103(a) over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi (U.S. Pat. No. 6,921,980).

Claim 1

Claim 1 is directed to an integrated circuit chip. The chip includes a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A second contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride. A first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening. A second opening in said passivation layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening. A power metal structure is over said passivation layer and on said first contact point. The power metal structure is connected to said first contact point through said first opening. The power metal structure comprises a copper layer. The power metal structure has a first region configured to be wirebonded thereto for connection made to a next level of packaging. A ground metal structure is over said passivation layer and on said second contact point. The ground metal structure is connected to said second contact point through said second opening. The ground metal structure comprises a copper layer. The ground metal

structure has a second region configured to be wirebonded thereto for connection made to said next level of packaging. A capacitor is over said passivation layer, vertically over said power and ground metal structures and vertically over said first contact point. A first solder joint is vertically over said first contact point and between a first terminal of said capacitor and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure. A second solder joint is between a second terminal of said capacitor and said ground metal structure, wherein said second solder joint connects said second terminal to said ground metal structure.

The Office Action equates Lin's capacitor 54 to the claimed capacitor recited in Claim 1 of the present application. *See,* Office Action, page 4, lines 5-6. Applicant respectfully disagrees. As recited in amended Claim 1 of the present application, a capacitor is provided vertically over a first contact point, which is at a bottom of an opening in a passivation layer. Thereby, the capacitor has a minimum path to the IC metal of a chip under the passivation layer. The capacitor can thereby immediately provide power to an activated active circuit before the power provided through wirebonded wires is delivered to the activated active circuit. *See, e.g.,* paragraph [0031] of the present application. As a result, an improved performance can be achieved by the arrangement disclosed in the present application. However, the Office Action does not provide any arguments that Lin's capacitor 54 is provided in such a position relative to the IC metal of a chip to perform such a function.

Furthermore, the Office Action concedes that Lin does not teach "a region used to be wirebonded thereto for connection made to a level of packaging." *See,* Office Action, page 4, lines 18-21. Therefore, the Office Action does not hold that Lin's capacitor 54 is to be connected to an external circuit through wirebonded wires. The Office Action cites Nakanishi's capacitor 8 as teaching such an arrangement. *See,* Office Action, page 4, line 21 to page 5, line 4. However, Nakanishi's capacitor 8 is disclosed to have two terminals connected to an external circuitry through the wiring traces 5. Nakanishi's capacitor 8 has terminals that are horizontally offset from the electrode pad 3; that is, Nakanishi's capacitor 8 is not located vertically over the electrode pad 3, but is connected to the electrode pad 3 through the wiring trace 25. Therefore, Nakanishi's capacitor 8 has a longer path to the IC metal of a chip than the claimed capacitor provided vertically over the claimed first contact point of the present application. Therefore,

Nakanishi's capacitor 8 is not seen to provide power for the activated active circuit so immediately before the power provided through Nakanishi's wiring trace 25 is delivered to the activated active circuit. It is therefore respectfully submitted that the Office Action has not established that one skilled in the art would be motivated to combine Lin and Nakanishi to arrive at a capacitor that is "over said passivation layer, vertically over said power and ground structures and vertically over said first contact point," as recited in amended Claim 1 of the present application.

In view of the above arguments, Claim 1 is believed to be patentable over the applied references. Reconsideration and withdrawal of the 35 U.S.C. § 103 rejection of Claim 1 are respectfully requested.

Claim 9

Claim 9 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer. A capacitor is over said passivation layer and over said second contact pad. A solder joint is between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad. A third contact pad between said solder joint and said second contact pad, wherein said third contact pad comprises electroplated copper, wherein a contact area between said third contact pad and said second contact pad is horizontally offset from said first contact point.

The Office Action considers that the claimed feature of the thickness of first gold layer being greater than 1 micrometer, recited in Claim 9, is considered to involve routine optimization. *See,* Office Action, page 10, lines 19-22. In particular, the Office Action states that Shirasaki (U.S. Pat. Pub. No. 2003/0043558) teaches a gold layer that has a thickness greater

than 1 micrometer (page 4, ¶ [0052] of Shirasaki). *See,* Office Action, page 22, lines 17-20. Applicant respectfully disagrees with the Office Action's broad interpretation of Shirasaki's gold layer.

Shirasaki teaches that "a metal such as nickel and gold, …, may be adhered to 0.01-20 μm in thickness by a plating method." *See,* Shirasaki, ¶[0052], lines 15-19. However, the teaching is not analogous to the claimed subject matter that a gold layer has a thickness greater than 1 micrometer, at least because a gold layer, as recited in Claim 9 of the present application, is not identical to a metal having a combination of nickel and gold, as disclosed by Shirasaki.

The Office Action further cites Arvin (U.S. Pat. Pub. No. 2003/0080092) as teaching that "the thickness of the various layers may vary widely but that gold layer is typically 0.03 to 2 microns, which includes applicant's recited range of gold layer." *See,* Office Action, page 24, line 19 to page 25, line 4.

However, Arvin's gold layer 14 is believed not be non-analogous to the first gold layer recited in Claim 9 of the present application at least because Arvin's gold layer 14 has different functions from the first gold layer recited in Claim 9 of the present application. For example, Arvin's gold layer 14 is finished to be bonded with a solder ball 17. However, the first gold layer of a second contact pad, as recited in Claim 9, is not finished to be bonded with a solder joint, but a third contact pad is provided between the solder joint and the second contact pad.

The Office Action also considers that even though electroplated copper, as recited in Claim 9, may have different microstructure than generic copper, the product in the product-by-process claims is obvious from a product of the prior art. *See,* Office Action, page 24, lines 1-4. Applicant respectfully disagrees.

The elements formed by different processes are believed to be not analogous to each other at least because different processes are not replaceable with each other when they form something in different locations or on different interfaces. Particularly, Claim 9 is amended with the claim feature that the third contact pad, between a solder joint and the second contact pad comprising a first gold layer with a thickness greater than 1 micrometer, comprises electroplated copper, which is not seen to be taught by Lin or Nakanishi. It is respectfully submitted that the

Office Action has not established that the combination of Lin and Nakanishi teaches or suggests the claimed arrangement recited in amended Claim 9.

Based on the above, it is respectfully submitted that Claim 9 is allowable over the applied references. Accordingly, reconsideration and withdrawal of the rejection of Claim 9 are respectfully requested.

Claim 15

Claim 15 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening. A third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point through said first opening and connected to said second contact pad, wherein said third contact pad has a region that is configured to be wirebonded thereto for connection made to a next level of packaging and is horizontally offset from said first contact point. A first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening. A capacitor over said first polymer layer and over said second contact point. A solder joint is between said second contact point and a terminal of said capacitor, wherein said solder joint connects said terminal to said second contact point.

The Office Action considers that the combination of Lin and Nakanishi teaches the claimed "third contact pad" feature recited in Claim 15 of the present application. *See,* Office Action, page 15, line 11 to page 16, line 9. Without addressing the merits of the Office Action's rejection of Claim 15, it is respectfully submitted that amended Claim 15 recites that "said third contact pad has a region that is configured to be wirebonded thereto for connection made to a

next level of packaging and is horizontally offset from said first contact point." It is believed that the applied references do not teach or suggest such a claimed feature of the third contact pad.

Based on the above, it is respectfully submitted that Claim 15 is allowable over the applied references. Accordingly, reconsideration and withdrawal of the rejection of Claim 15 are respectfully requested.

Claim 129

Claim 129 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer. A capacitor is over said passivation layer and over said second contact pad. A solder joint between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad. A third contact pad is between said solder joint and said second contact pad, wherein said third contact pad is finished with a solder wettable material comprising gold, wherein a contact area between said third contact pad and said second contact pad is horizontally offset from said first contact point.

For similar reasons as those discussed above with respect to Claim 9 regarding "a first gold layer" and "a third contact pad" claim features, Claim 129 is also believed to be allowable over the applied references. Accordingly, reconsideration and withdrawal of the rejection of Claim 129 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed

to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicant submits that the claims are in condition for allowance and respectfully request a notice to this effect.

Should the Examiner have any questions, the Examiner is invited to call the undersigned. All correspondence should be directed to our address given below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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